

## Quad 2-input EXCLUSIVE-OR gate

## 74LVC86A

## FEATURES

- 5 V tolerant inputs, for interfacing with 5 V logic
- Supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltage up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

## DESCRIPTION

The 74LVC86A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC86A provides the 2-input EXCLUSIVE-OR function.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nA, nB to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.0	ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	20	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

## Note

1. H = HIGH voltage level;  
L = LOW voltage level.

## Quad 2-input EXCLUSIVE-OR gate

74LVC86A

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC86AD	-40 to +125 °C	14	SO14	plastic	SOT108-1
74LVC86ADB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74LVC86APW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74LVC86ABQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V <sub>CC</sub>	supply voltage

Quad 2-input EXCLUSIVE-OR gate

74LVC86A

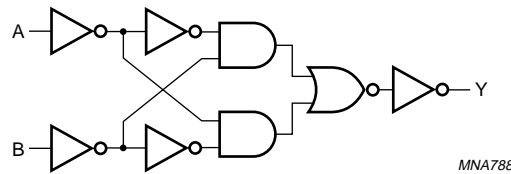


Fig.5 Logic diagram (one gate).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage		0	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	note 1	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO14 packages: above 70 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.  
 For (T)SSOP14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.  
 For DHVQFN14 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 4.5 mW/K.

## Quad 2-input EXCLUSIVE-OR gate

## 74LVC86A

**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -100 µA	2.7	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	-	GND	0.20	V
		I <sub>O</sub> = 100 µA	2.7	-	-	0.40	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	±0.1	±5	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	5	500	µA

## Quad 2-input EXCLUSIVE-OR gate

## 74LVC86A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	V <sub>CC</sub> – 0.3	–	–	V
		I <sub>O</sub> = –100 µA	2.7	V <sub>CC</sub> – 0.65	–	–	V
		I <sub>O</sub> = –12 mA	3.0	V <sub>CC</sub> – 0.75	–	–	V
		I <sub>O</sub> = –18 mA	3.0	V <sub>CC</sub> – 1.0	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	–	–	0.3	V
		I <sub>O</sub> = 100 µA	2.7	–	–	0.6	V
		I <sub>O</sub> = 12 mA	3.0	–	–	0.8	V
		I <sub>O</sub> = 24 mA					
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	–	±20	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	–	40	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	–	5000	µA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

Quad 2-input EXCLUSIVE-OR gate

74LVC86A

AC CHARACTERISTICS

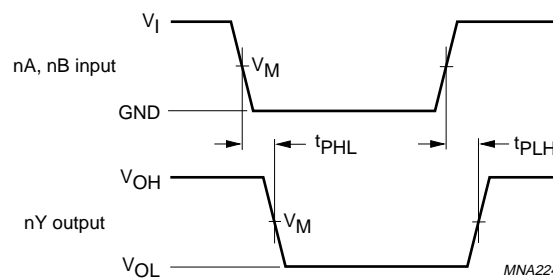
GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	11	–	ns
			2.7	1.0	3.4	5.8	ns
			3.0 to 3.6	1.0	3.0 <sup>(2)</sup>	5.0	ns
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	1.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.0	–	9.0	ns
			3.0 to 3.6	1.0	–	6.5	ns
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	1.5	ns

Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. This typical value is measured at V<sub>CC</sub> = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



V<sub>M</sub> = 1.5 V at V<sub>CC</sub> ≥ 2.7 V.  
 V<sub>M</sub> = 0.5V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V.  
 V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 The inputs nA and nB to output nY propagation delay.

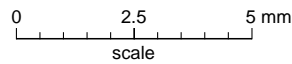
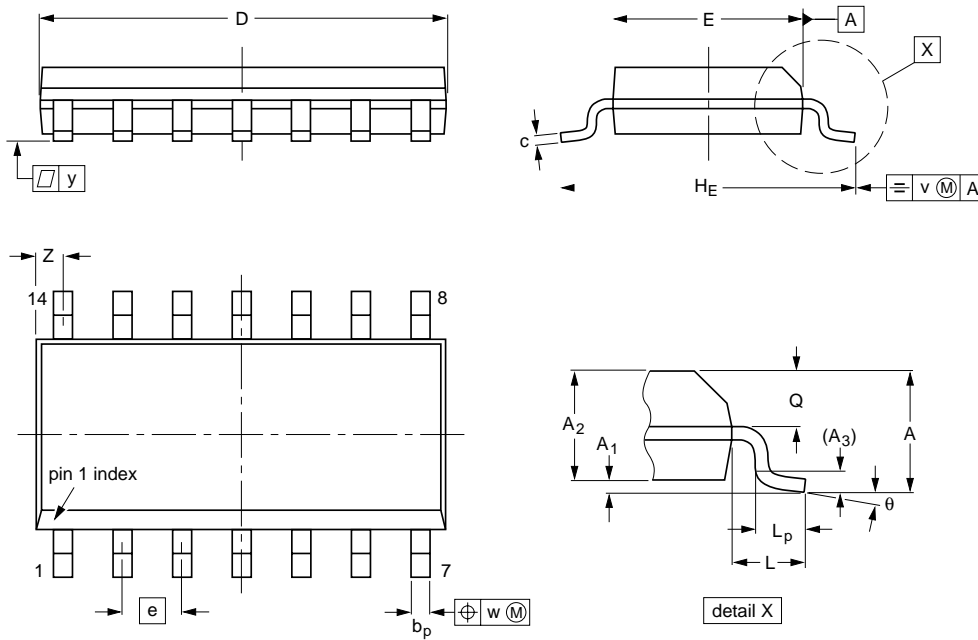
Quad 2-input EXCLUSIVE-OR gate

74LVC86A

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION
	IEC	JEDEC	JEITA	
SOT108-1	076E06	MS-012		